8. A silicon carbide semiconductor device comprising:
a substrate made of silicon carbide, the substrate having one of a first conductivity type and a second conductivity type, the substrate having first and second opposing surfaces;
a drift layer located on the first surface of the substrate, the drift layer made of silicon carbide, the drift layer having the first conductivity type and having an impurity concentration less than an impurity concentration of the substrate;
a trench provided from a surface of the drift layer;
a base region sandwiching the trench so as to be in contact with a sidewall of the trench, the base region made of silicon carbide and having the second conductivity type;
a source region located on the base region and sandwiching the trench, the source region being in contact with the sidewall of the trench, the source region made of silicon carbide, the source region having the first conductive type and having an impurity concentration greater than the impurity concentration of the drift layer;
a gate insulating layer located on a surface of the trench;
a gate electrode located on the gate insulating layer in the trench;
a source electrode electrically coupled with the source region and the base region;
a drain electrode located on the second surface of the substrate; and
a deep layer located under the base region and extending to a depth deeper than the trench, the deep layer formed along an approximately normal direction to the sidewall of the trench, the deep layer having the second conductivity type, wherein
an inversion channel is provided at a surface portion of the base region located on the sidewall of the trench and electric current flows between the source electrode and the drain electrode through the source region and the drift layer by controlling a voltage applied to the gate electrode.

9. A silicon carbide semiconductor device comprising:
a substrate made of silicon carbide, the substrate having one of a first conductivity type and a second conductivity type, the substrate having first and second opposing surfaces;
a drift layer located on the first surface of the substrate, the drift layer made of silicon carbide, the drift layer having the first conductivity type and having an impurity concentration less than an impurity concentration of the substrate;
a base region located on the drift layer, the base region made of silicon carbide and having the second conductivity type;
a source region located on the base region, the source region made of silicon carbide, the source region having the first conductive type and having an impurity concentration greater than the impurity concentration of the drift layer;
a trench extending to a depth deeper than the source region and the base region and reaching the drift layer, the trench sandwiched by each of the base region and the source region, the trench provided along a first direction;
a gate insulating layer located on a surface of the trench;
a gate electrode located on the gate insulating layer in the trench;
a source electrode electrically coupled with the source region and the base region;
a drain electrode located on the second surface of the substrate;
a deep layer located under the base region and extending to a depth deeper than the trench, the deep layer formed in parallel with a planer direction of the substrate along a second direction crossing the first direction, the deep layer having the second conductivity type; and
a body layer having a predetermined distance from a sidewall of the trench, the body layer located at a portion deeper than the source region, the body layer having the second conductivity type and having an impurity concentration greater than the impurity concentration of the base region, wherein
an inversion channel is provided at a surface portion of the base region located on the sidewall of the trench and electric current flows between the source electrode and the drain electrode through the source region and the drift layer by controlling a voltage applied to the gate electrode.

10. The silicon carbide semiconductor device according to claim **9**, further comprising one or more of the deep layers, wherein:
each of the deep layers has a width of about 1.5 μm;
the deep layers are arranged at intervals of about 2.0 μm; and
the predetermined distance from the sidewall of the trench and the body layer is between about 0.4 μm and about 0.9 μm.

11. The silicon carbide semiconductor device according to claim **9**, wherein
the impurity concentration of the base region is between about 5.0×10^{15} cm^{-3} and about 5.0×10^{16} cm^{-3}; and
the impurity concentration of the body layer is between about 1.0×10^{18} cm^{-3} and about 1.0×10^{20} cm^{-3}.

12. A silicon carbide semiconductor device comprising:
a substrate made of silicon carbide, the substrate having one of a first conductivity type and a second conductivity type, the substrate having first and second opposing surfaces;
a drift layer located on the first surface of the substrate, the drift layer made of silicon carbide, the drift layer having the first conductivity type and having an impurity concentration less than an impurity concentration of the substrate, the drift layer having a cell section and a peripheral section surrounding the cell section;
a base region located on the cell section of the drift layer, the base region made of silicon carbide and having the second conductivity type;
a source region located on the base region, the source region made of silicon carbide, the source region having the first conductive type and having an impurity concentration greater than the impurity concentration of the drift layer;
a plurality of trenches extending to a depth deeper than the source region and the base region and reaching the drift layer, the plurality of trenches arranged in a stripe pattern, each of the plurality of trenches sandwiched by each of the base region and the source region, each of the plurality of trenches provided along a first direction;
a gate insulating layer located on a surface of each of the plurality of trenches;